Fabrication of patterned sapphire substrate and effect of light emission pattern on package efficiency

Xu-Fong Li,[1] Shih-Wei Huang,[1] Hong-Yu Lin,[1] Chun-Yan Lu,[2] Shang-Fu Yang,[2] Ching-Cherng Sun,[2] and Cheng-Yi Liu[1*]

[1]*Department of Chemical Engineering and Materials Engineering, National Central University, Chungli 32001, Taiwan*

[2]*Institute of Lighting and Display Science/Department of Optics and Photonics, National Central University, Chungli 32001, Taiwan*

**ChengyiLiuOEM@gmail.com*

Abstract: Pyramidal nature PSS (n-PSS) substrates were produced by a simple wet etching process without standard lithography and dry-etching processes. We found that the output power of the LED on the pyramidal n-PSS substrates is larger than the output power of the LED chip on the flat c-plane sapphire substrate by 46.4% to 51.5%. LED chip on the n-PSS(III) substrate with 73% pattern coverage has the highest output power among LED chips on all n-PSS substrates. The light emission patterns of LED bare chips on different n-PSS and r-PSS substrates were studied. The shape of the light emission pattern was qualitatively defined by the broadness angle, which is the angle at the maximum intensity of the light emission pattern away from the normal direction. The broadness angle is inversely proportional to the facet angle of pyramids created on the n-PSS substrates. In addition, we found that the light extraction efficiency at the GaN/silicone interface has a dependence on the light emission pattern of the bare chips on different n-PSS substrates. The broader light emission pattern (larger broadness angle) would result in higher light extraction efficiency at the GaN/silicone interface.

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1. Introduction

As the luminous efficiency of GaN-based LED has been improving continuously, GaN-based LEDs are replacing the traditional tungsten lamps as the general lighting source. To further improve the luminous efficiency of GaN-based LEDs, people have been putting great effort in two major areas, which are the external quantum efficiency of the GaN LED chip emitter and the efficiency of the white-light package on GaN LED chip [1–5]. In recent years, patterned sapphire substrate (PSS) has become the main trend for the sapphire substrates used for growing the MOCVD GaN LED expitaxial layers [6,7]. The patterns on the PSS wafers would result in epitaxial lateral overgrowth (ELOG) during the MOCVD GaN epi-layers growth, which effectively reduces the formation of dislocations at the GaN/sapphire interface. It has been widely reported that the PSS wafers can improve the internal quantum efficiency by 50% at least [8].

In addition to the improvement in the internal quantum efficiency, the patterns on the PSS wafers also can improve the light extraction efficiency of the GaN LED chips [9,10]. It is known that the total internal reflection (TIR) at the emitting interface of GaN LED chip is the main issue limiting the light extraction efficiency. Based on Snell's law, the critical TIR angle at the GaN/air interface is only 23.58°. So, a large portion of the light emitted at the active layers would be trapped in GaN-based LED.

The pattern created on the PSS wafers would destroy the TIR effect at the emitting interface, so, more light can be extracted out to the outer ambient. Hence, the light extraction efficiency at the emitting interface would be enhanced.

The current commercial PSS wafers are fabricated by the lithography technique and the dry etching technologies [11]. In this work, we produce PSS wafers without using lithography and dry etching processes. We produced PSS wafers by using a simple wet etching process. Pyramidal pattern simultaneously form on the c-plane flat sapphire substrates. The produced PSS wafers with pyramidal pattern in this work are defined as nature PSS (n-PSS). Besides, a commercial PSS wafer with regular array pattern (r-PSS) was added into the present work for the comparison purpose.

2. Experimental

The fabrication processes of the n-PSS wafers are described in the following. Before the wet etching process, a PECVD (Plasma Enhanced Chemical Vapor Deposition) SiO_2 layer was deposited on the back-side of the c-plane sapphire wafers to prevent the back-side of the sapphire from being etched. The flat back-side of the pattern sapphire wafers provides good contact with the growth plate in the MOCVD chamber, which ensures good quality during the MOCVD epitaxial process. Then, the sapphire wafers were immersed into pure H_2SO_4 solution for the sapphire etching process and the etching temperature was controlled at a constant temperature of 250 °C. After MOCVD process, GaN LED epitaxial structure was grown on the sapphire wafers with the pyramidal pattern. The LED epi-layer structure includes a 1.8 μm thick undoped GaN layer and a 2.5 μm thick Si-doped n-type GaN cladding layer, an active region with six periods of InGaN/GaN multiple quantum wells (MQWs), and a 0.3 μm thick Mg-doped p-type GaN cladding layer. The schematic of the GaN LED is shown as the Fig. 4(a). For simplicity, there is no mirror on the back side of the LED chips. Also, the wavelength of all LEDs is very close, within 5 nm difference.

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3. Results and discussion

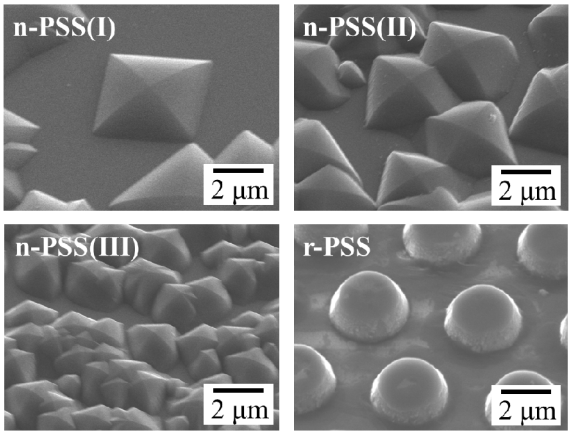

Fig. 1. Pattern morphology on n-PSS and r-PSS wafers.

The pattern morphology on the three n-PSS wafers is shown in Fig. 1. The main pattern morphology on the n-PSS wafers is the four-sides pyramid. The average size of the pyramids on the n-PSS(I), n-PSS(II), n-PSS(III), and r-PSS wafers is about 4.8 μm, 4 μm, 2.2 μm, and 3μm, respectively. Also, we note that the dihedral angle between the side-planes of the pyramids and the c-plane of the sapphire wafer depends on the size of the pyramids on the n-PSS wafers. The dihedral angles of the pyramids on n-PSS(I), n-PSS(II), and n-PSS(III) substrate are estimated to be 24.5°, 32.1°, and 45.4 °. All the information about the pyramidal pattern on n-PSS and r-PSS wafers is tabulated in Table 1. And, the coverage percentage of the pyramidal pattern on the n-PSS(I), n-PSS(II), n-PSS(III), and r-PSS substrates can be estimated by the top-view SEM images. The coverage percentages of the pyramidal pattern of the n-PSS(I), n-PSS(II), n-PSS(III), and r-PSS substrates are estimated to be 53%, 65.8%, 73%, and 39.9%, respectively. We found that the n-PSS substrate with a smaller pattern size has a larger pattern coverage on the n-PSS wafers. In addition, a flat c-plane sapphire substrate (f-SS) was taken to study for the comparison purpose in this work.

Table 1. Characters of pattern morphology and GaN epi-layers on n-PSS, r-PSS, and f-SS wafers

Symbol	Pattern size(μm) /Coverage (%)	Dihedral angle (°)	XRD FWHM at (002)	Residual stress (M Pa)	Δθ (°)
n-PSS I	(5 / 53)	24.5	0.0349	–694	42.5
n-PSS II	(4 / 65.8)	32.1	0.0341	–861	38
n-PSS III	(2 / 73)	45.4	0.0339	–861	32
r-PSS	(3/39.9)	58.6	0.0333	–663	37.5
f-SS	-	-	0.0413	–611	37

A. MOCVD-grown GaN epi-layers on n-PSS and r-PSS wafers

GaN LED epitaxial structure was grown on the five sapphire substrates (n-PSS(I), n-PSS(II), n-PSS(III), r-PSS, and f-SS) by MOCVD growth process. After the MOCVD epitaxial process, the MOCVD-grown GaN epi-layers were analyzed by XRD. The full width at half maximum (FWHM) of the (002) diffraction peak implies the degree of the dislocation density in the MOCVD-grown GaN epi-layers. The FWHM values of MOCVD-grown GaN epi-layers on the five sapphire substrates (n-PSS(I), n-PSS(II), n-PSS(III), r-PSS, and f-SS) are tabulated in Table 1. In general, the GaN epi-layers on PSS wafers (n-PSS and r-PSS) have a smaller FWHM value than that of the GaN epi-layer grown on the flat substrate. In addition, we note that value of FWHM decreases with the pattern coverage of the n-PSS wafers. The

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above two findings suggest that the pyramidal pattern on PSS wafers can indeed reduce the dislocation density in the GaN epi-layers.

The residual stress in the GaN epi-layers is another important issue, which affects the internal quantum efficiency of the GaN LED epi-layers [12]. How does the pyramidal pattern on the n-PSS wafers influence the residual stress of the GaN epi-layers has never been studied. The residual stress in the GaN epi-layers can be measured by the high-E2 mode peak position in Raman spectrum [12]. The residual stress (σ_{GaN}) can be estimated through the modified Kozawa equation:

$$(P - 566.5) = -3.6 \cdot \sigma_{GaN}, \quad (1)$$

where P stands for the high-E2 mode peak position in Raman spectrum and 566.5 is the high-E2 mode peak position in Raman spectrum of a stress-free GaN.

The residual compressive stress in the GaN epi-layers is mainly contributed by the CTE mismatch between the sapphire substrate (7.5*10-6/K) and the GaN (5.5*10-6/K) epi-layers. As the MOCVD-grown GaN epi-wafer cools down from the epitaxial temperature (about 1100°) to room temperature, the sapphire substrate would contract more than the GaN epi-layers and exert a compressive force on the GaN epi-layers. Therefore, a compressive residual stress would be resulted in the MOCVD-grown GaN epi-layers. The residual compressive stress of the GaN epi-layers on the n-PSS(I), n-PSS(II), n-PSS(III), r-PSS and f-SS substrates is listed in Table 1. We found that the GaN epi-layers on the PSS wafers has a higher residual compressive stress than that on the f-SS wafer. And, the GaN epi-layer on the PSS substrate with a higher pattern coverage has a larger compressive stress.

As mentioned previously, the compressive stress of the GaN epi-layer comes from the contraction of the sapphire substrate, as the GaN epi-wafer cools down to room temperature from the MOCVD growth temperature. Thus, the coverage of the sapphire pattern would determine the contraction force acted on the GaN epi-layers. Another possible cause for the increase in stress of the GaN epi-layers on the PSS with the highest pattern coverage is due to the differences in the rates of contraction of the GaN epi-layers and the sapphire, which contains a component parallel to the c-axis for epitaxy grown on the pyramid sides. Therefore, a higher density of pyramidal structures will inevitably introduce more strain. This explains that the GaN epi-layer on the n-PSS substrates has a larger compressive stress than that on the f-SS wafer. Also, as seen in Table 1, the compressive stress in the GaN epi-layer on the n-PSS wafers with a higher pattern coverage is larger than the compressive stress in the GaN epi-layers on the n-PSS wafer with a less pattern coverage. This is also because that the n-PSS wafers with a higher pattern coverage have more GaN/sapphire interface area, which results in a larger compressive stress in the GaN epi-layers. The above analysis justifies the stress measurement of the GaN epi-layers on the n-PSS, r-PSS, and f-SS wafers shown in Table 1.

All MOCVD-grown GaN LED epi-layers on n-PSS(I), n-PSS(II), n-PSS(III), r-PSS, and f-SS wafers were processed to 1000 μm ∗ 1000 μm conventional horizontal LED chips. The forward voltages of all LED chips on n-PSS(I), n-PSS(II), n-PSS(III), r-PSS, and f-SS were measured to be 3.35 V, 3.35 V, 3.34 V, 3.19 V, and 3.21 V, respectively, at an injection current of 350 mA. The pattern on n-PSS wafers would slightly affect the electrical property of LED chips.

Figure 2 shows the light output power of LED bare chips on the five sapphire substrates at an injection current of 350 mA. In general, the output power of LED chips on patterned sapphires (n-PSS(I), n-PSS(II), n-PSS(III), and r-PSS) is larger than that of the LED chip on the f-SS wafer by 46.7%~59.7%. Among the LED chips on all PSS wafers, the LED chips on the n-PSS(III) wafer have the highest output power. Interestingly, we found that the output power of the LED chips on the n-PSS(III) wafer is even larger than that of the LED chips on the commercial r-PSS wafer.

It should be due to that the n-PSS(III) wafer has the highest pattern coverage among the studied PSS wafers. The high pattern coverage can improve epitaxial quality of the GaN epi-

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layers and the internal quantum efficiency of LED chips [10]. This is also can be verified by the previous FWHM values of the GaN epi-layer on n-PSS wafers, shown in Table 1.

The light output power of LED bare chips (external quantum efficiency) on the five sapphire substrates depends on both internal quantum efficiency and light extraction efficiency. It is known that the total internal reflection (TIR) effect is the main issue limiting the light extraction efficiency of the LED chip. The pattern on PSS wafers could effectively mitigate TIR effect. So, in addition to the improvement in internal quantum efficiency, the high pattern coverage on the n-PSS(III) wafer could enhance light extraction efficiency as well. Thus, the high pattern coverage on the n-PSS(III) wafer is the key for the highest light output power among the LED chips on the studied n-PSS wafers.

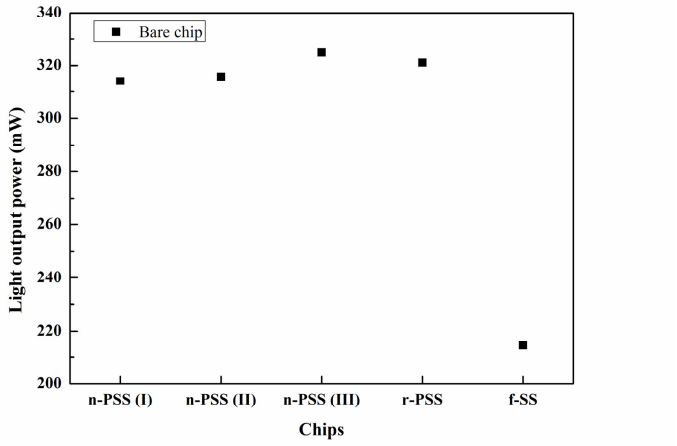

Fig. 2. Output power of LED bare chips on n-PSS, r-PSS, and f-SS wafers.

B. Effect of emission light pattern on light extraction efficiency

The light emitted from LED chip is not uniform in direction. There is a spatial distribution in the emitting intensity of a single LED chip, which is defined as the light emission pattern in this study. The typical light emission pattern of current LED chip has a lambertian distribution, as shown in Fig. 3(a). Figures 3(b)-3(f) show the light emission patterns of LED chips on five sapphire substrates. As shown in Fig. 3, the maximum intensity of the light emission patterns of LED chips on five sapphire substrates all occurs at the side-angle range. For example, the maximum intensity of the LED chip on the n-PSS(I) wafer locates at about 42.5°, as seen in Fig. 3(b). We define the average angle at the maximum intensity of the light emission pattern away from the normal direction as the broadness angle ($\Delta\theta$), as shown in Fig. 3. The broadness angles of LED chips on five sapphire substrates are measured and tabulated in Table 1. As seen in Table 1, we can see that the broadness angle is inversely proportional to the dihedral angle (the angle between the side-plane of the pyramids and the c-plane of the sapphire substrates).

Note that, to be used as the white-light source, the GaN LED chips need to be packed with the white-light LED package. How does the light emission pattern of bare LED chips affect the efficiency of the white-light LED package is an important issue to investigate. To study this problem, we first review the white-light LED package process in the following: LED chips are die-attached on the ceramic substrates. The ceramic substrates are bonded with the secondary aluminum heat-dissipation substrates. The die-attached LED chips were encapsulated with silicone mixed with YAG:Ce phosphor. The entire white-light LED package structure is sketched in Fig. 4(b). Yellow region represents the phosphor region, i.e., silicone mixed with YAG:Ce phosphor. The diameter of the phosphor region is about 3 mm.

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Then, a silicone lens was used to cap the phosphor region. The diameter of the entire silicone lens is 6 mm. YAG:Ce phosphors absorb the blue light emitted from LED chips and radiate yellow light, which combines with un-converted blue light to yield white light.

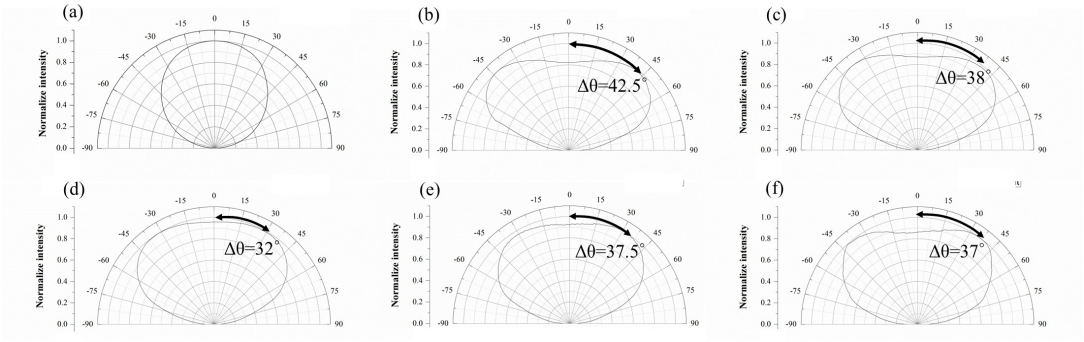

Fig. 3. (a) the Lambertian distribution and the light emission pattern of LED bare chips on (b) n-PSS (I) (c) n-PSS (II) (d) n-PSS (III) (e) r-PSS (f) f-SS.

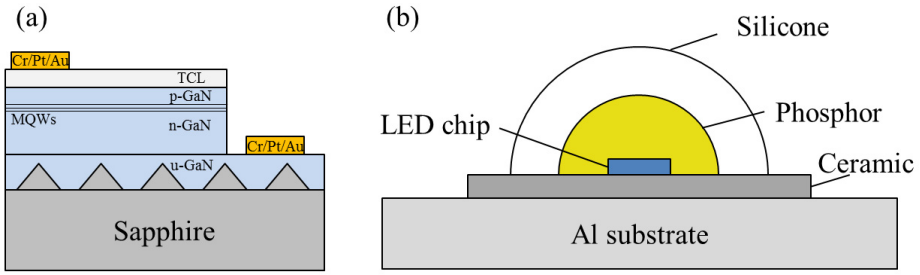

Fig. 4. (a) The structure of the GaN LED (b). White-light LED package structure.

People have been aware that, as the light emitted from the LED chips enters into the outer ambient, the TIR effect would occur at the emitting interface. Using the GaN LED bare chip as example, as the emitting light travels from the GaN epi-layer into air medium, the TIR effect would occur at the GaN/air interface. With knowing the refractive index of GaN (n = 2.5) and air (n = 1), the critical TIR angle (23.58°) at the GaN/air interface can be calculated by using Snell's law. It implies that the emitting light with an incident angle at the GaN/air interface large than 23.58° cannot be extracted into air. After being encapsulated with silicone, the critical TIR angle between GaN (n = 2.5) and silicone (n = 1.41) increases to 34.33°. It means that the light extraction efficiency at the LED emitting interface (i.e., GaN/silicone interface) could be enhanced by the silicone encapsulation. In the present work (Fig. 3), we have realized that the light emission pattern of the bare chips depends on the pattern morphology on the n-PSS substrates. So, an important issue needing to be understood is that how does the shape of the light emission pattern affect the light extraction at the GaN/silicone interface.

To evaluate the above issue, two pieces of information have to be obtained. They are (1) the light output power of the bare LED chips (P_{bare}) and (2) the light output power ($P_{inside-silicone}$) inside the silicone emitted from the LED chips. Then, the light extraction efficiency ($LEE_{GaN/silicone}$) at the GaN/silicone interface can be expressed as:

$$LEE_{GaN/Silicone} = P_{inside-silicone} / P_{Bare} \quad (2)$$

However, $P_{inside-silicone}$ cannot be measured directly. An indirect approach to access the value of the light output power ($P_{inside-silicone}$) inside the silicone is described below. Firstly, the effect of YAG:Ce phosphor has to be removed. So, all LED bare chips on different n-PSS

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substrates were packaged with silicone lens only, i.e., without YAG:Ce phosphor. Then, the output power ($P_{ouside\text{-}silicone}$) of these silicone-only-packaged LED chips were measured and tabulated in Table 2. The output power ($P_{ouside\text{-}silicone}$) is larger than the output power (P_{bare}) of the bare LED chips. The light output power improvement after silicone encapsulation should be owing to the enhancement in the light extraction efficiency ($LEE_{GaN/silicone}$) at the GaN/silicone interface.

We note that the emitted light inside the silicone ($P_{inside\text{-}silicone}$) has to go through two processes to be detected as the output power ($P_{ouside\text{-}silicone}$) out of silicone lens. Firstly, the light inside the silicone has to across the silicone/air interface. So, again, TIR effect could happen at the silicone/air interface. The encapsulating lens is semi-spherical shape, so, the emission light from the LED chips can be regarded as to be always normal at the silicone/air interface. Even if the emission light normally passes through the silicone/air interface, the TIR effect still could not be ignored. Besides TIR effect at the silicone/air interface, the loss in Fresnel loss and photon recycle also have to be considered, as the emitted light travel in the silicone lens. By using Monte-Carlo ray tracing method (Advanced Systems Analysis Program), Sun simulated the loss percentage due to the TIR effect, Fresnel loss and photon recycle, as the emitted light travel through the silicone lens [5]. They reported that the lost percentage due to the Fresnel loss and photon recycle is about 1.4%. Thus, the output power of $P_{outside\text{-}silicone}$ would be the light output power inside the silicone lens ($P_{inside\text{-}silicone}$) times 0.986, i.e., (1 – 0.014). It means that the light output power ($P_{inside\text{-}silicone}$) inside the silicone lens could be expressed as:

$$P_{inside-silicone} = P_{outside-silicone} / 0.986 \tag{3}$$

The output power of $P_{outside\text{-}silicone}$ has been measured and shown in Table 2. Thus, the output power ($P_{inside\text{-}silicone}$) of the light inside the silicone lens can be deduced out by Eq. (3). The magnitudes of $P_{inside\text{-}silicone}$ of LED chips on different n-PSS substrates and r-PSS are tabulated in Table 2. With knowing the output power ($P_{inside\text{-}silicone}$) of the light inside the silicone lens, the light extraction efficiency ($LEE_{GaN/silicone}$) at the GaN/silicone interface can be obtained by the Eq. (2). $LEE_{GaN/silicone}$ values of LED chips on diffferent n-PSS and r-PSS substrates are listed in Table 2.

Table 2. light output powers of LED chips on n-PSS, r-PSS and f-SS wafers

Symbol	P_{bare} (mW)	$P_{inside\text{-}silicone}$ (mW)	$P_{outside\text{-}silicone}$ (mW)	$LEE_{GaN/silicone}$ (%)
n-PSS I	314	474.1	467.3	151
n-PSS II	315.7	473.6	465.4	150
n-PSS III	325	474.5	466.3	146
r-PSS	321.1	475.2	467	148
f-SS	214.5	345.3	341.4	161

From the above analysis, we can conclude that the light extraction efficiency ($LEE_{GaN/silicone}$) at the GaN/silicone interface has a dependence on the light emission pattern of the bare chips on different n-PSS and r-PSS substrates. Figure 5 plots $LEE_{GaN/silicone}$ against $\Delta\theta$. Interestingly, we found that $LEE_{GaN/silicone}$ roughly increases with $\Delta\theta$. In the other words, the broader light emission pattern (larger $\Delta\theta$) would result in the higher light extraction efficiency ($LEE_{GaN/silicone}$) at the GaN/silicone interface.

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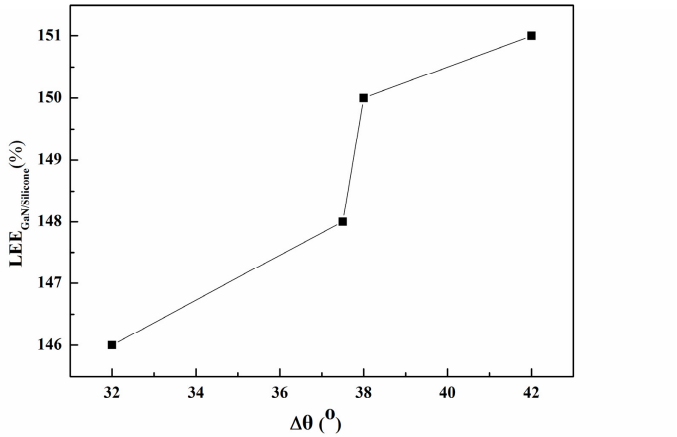

Fig. 5. Light extraction efficiency ($LEE_{GaN/silicone}$) at the GaN/silicone interface against broadness angle (Δθ).

4. Conclusions

In summary, three n-PSS substrates were produced by a simple wet etching process without standard lithography and dry-etching processes. The studied n-PSS and r-PSS wafers can enhance the output power of the LED by 46.4% ~51.5%, compared to the output power of the LED chip on the flat c-plane sapphire substrate (f-SS wafer). LED chip on the n-PSS(III) wafer with 73% pattern coverage has the highest output power among LED chips on all PSS wafers.

We also studied the light emission pattern of LED bare chips on different n-PSS wafers and r-PSS wafer. We quantitize the broadness of the light emission pattern by measuring the angle at the maximum intensity of the light emission pattern away from the normal direction as the broadness angle (Δθ). The broadness angle (Δθ) is inversely proportional to the facet angle of pyramids created on the n-PSS wafers.

At last, we found that the light extraction efficiency ($LEE_{GaN/silicone}$) at the GaN/silicone interface has a dependence on the light emission pattern of the bare chips on different PSS wafers. In addition, it can be concluded that the broader light emission pattern (larger Δθ), the higher light extraction enhancement efficiency ($LEE_{GaN/silicone}$) at the GaN/silicone interface.

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